OIPE
MAR 2 3 2007
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Chad A. Cobbley et al.	§	Group Art Unit:	2813
Serial No.: 10/770,919	§	Examiner:	Mitchell, James M.
Filed: February 3, 2004	§		
For: STACKED DIE MODULE AND TECHNIQUES FOR FORMING A STACKED DIE MODULE	§	Atty Docket:	MICS:0078-5/FLE (01-0752.05)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING
37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:

March 19, 2007 — Date
Jeanna Reed — Jeanna Reed

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on January 16, 2007, and received by the Patent Office on January 22, 2007.

Appellants hereby authorize the Commissioner to charge the fee of $500 for this Appeal Brief and any other fees that may be required to further prosecution to the credit card listed on the attached PTO-2038. However, if the PTO-2038 is missing, if the amount listed thereon is insufficient to further prosecution, or if the amount is unable to be charged to the credit card for any reason, the Commissioner is authorized to charge Deposit Account No. 06-1315; Order No. 01-0752.05/MAN (MICS:0078-5).

03/23/2007 FMETEKI1 00000031 10770919
01 FC:1402 500.00 OP

1. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc. the Assignee of the above-referenced application by virtue of the Assignment recorded on May 8, 2002 at reel 012905, frame 0018. Accordingly, the Assignee of the above-referenced application will be directly affected by the Board's decision in the pending appeal.

2. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellants' legal representative in this Appeal.

3. STATUS OF CLAIMS

Claims 1-21 are currently pending. Claims 3, 4 and 16-21 are withdrawn from consideration. Claims 1, 2 and 5-15 are currently under final rejection and, thus, are the subject of this Appeal.

4. STATUS OF AMENDMENTS

There are no outstanding amendments to be considered by the Board.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates generally to the field of semiconductor processing. Embodiments of the present technique are directed to forming a completed die stack on a temporary holding surface (e.g., a film frame, gel pack, tape reel, or JDEC tray) for later attachment to a substrate. *See* Application, page 12, lines 11-13.

The Application contains three independent claims, namely, claims 1, 10 and 16. As set forth above, claim 16 is withdrawn and claims 1 and 10 are the subject of this Appeal. The subject matter of claims 1 and 10 is summarized below. A benefit of the invention, as recited in these claims, is that the die stacks are formed on a temporary surface rather than forming the die stacks directly on a substrate or lead frame. *See*

Application, page 13, line 20 – page 14, line 2; page 17, line 16 – page 18, line 11. Thus, present embodiments facilitate later attachment of the plurality of die stacks to a substrate with one motion, thereby reducing the number of iterations as compared to the typical method of forming die stacks directly on the substrate. *See* Application, page 13, line 20 – page 14, line 2. Additionally, the die stack can be assembled using a first adhesive and cured at a different temperature than the adhesive later used to attach the die stack to a substrate, thus avoiding cracking and other related issues. *See* Application, page 13, line 20 – page 14, line 2; page 17, line 16 – page 18, line 11. Further, the die stack can be electrically, environmentally, structurally and/or functionally tested prior to attachment to a substrate. *See* Application, page 13, line 20 – page 14, line 2; page 17, line 16 – page 18, line 11. Indeed, by assembling the die stacks without prior attachment to a corresponding substrate, various reliability data can be gathered and failure mechanisms can be identified on the die stacks which may improve future design iterations, as well as prevent early failure of packages which have been incorporated into systems. *See* Application, page 13, line 20 – page 14, line 2; page 17, line 16 – page 18, line 11. After desired testing, the die stacks may be attached to a substrate to form a package. These are clear differences and distinctions from the prior art, as discussed below. *See* Application, page 13, line 20 – page 14, line 2; page 17, line 16 – page 18, line 11.

With regard to the aspect of the invention set forth in independent claim 1, discussions of the recited features of claim 1 can be found at least in the below cited locations of the specification and drawings. By way of example, embodiments of the present invention may comprise a holder (e.g., temporary holding surface 116 or wafers 104, 106, and 108) having a plurality of semiconductor die stacks (e.g., stacks 70, 80, and 90) thereon, the holder configured to temporarily hold the plurality of semiconductor die stacks. *See e.g.*, Application, page 12, line 10 – page 13, line 18; and FIGS. 4B, 4C, 5A, 5B, 5C, and 5D. Each of the plurality of die stacks may include at least two semiconductor die (e.g., dies 62, 64, 66, 72, 74, 76, 82, 84, 86, 92, 94, 96) coupled together by an adhesive and wherein the plurality of semiconductor die stacks do not include a lead frame or a substrate. *See e.g.*, Application, page 11, lines 4-8; page 12,

lines 1-10; page 13, lines 20-21; page 16, lines 9-23; page 17, lines 9-14; page 17, line 16 – page 18, line 11; and FIGS. 4B, 4C, and 6.

With regard to the aspect of the invention set forth in independent claim 10, discussions of the recited features of claim 10 can be found at least in the below cited locations of the specification and drawings. By way of example, embodiments of the present invention may comprise a tape reel (e.g., temporary holding surface 116) having a plurality of semiconductor die stacks (e.g., stacks 70, 80, and 90) thereon, the tape configured to temporarily hold the plurality of semiconductor die stacks. *See e.g.*, Application, page 12, line 10 – page 13, line 18; and FIGS. 4B, 4C, 5A, 5B, 5C, and 5D. Each of the plurality of semiconductor die stacks may include at least two semiconductor die (e.g., dies 62, 64, 66, 72, 74, 76, 82, 84, 86, 92, 94, 96) coupled together by an adhesive and wherein the plurality of semiconductor die stacks do not include a lead frame or a substrate. *See e.g.*, Application, page 11, lines 4-8; page 12, lines 1-10; page 13, lines 20-21; page 16, lines 9-23; page 17, lines 9-14; page 17, line 16 – page 18, line 11; and FIGS. 4B, 4C, and 6.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

First Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's first ground of rejection in which the Examiner rejected claims 1, 2, and 5-15 under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement.

Second Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's second ground of rejection in which the Examiner rejected claims 1, 2, and 5-15 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement.

Third Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's third ground of rejection in which the Examiner rejected claims 1, 2, and 5-15 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Fourth Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's fourth ground of rejection in which the Examiner rejected claims 1, 5-9, and 11 under 35 U.S.C. § 103(a) as being obvious over Sakurai (JP57015455) in view of Ang et al. (U.S. Patent No. 6,599,764).

Fifth Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's fifth ground of rejection in which the Examiner rejected claim 1 under 35 U.S.C. § 103(a) as being obvious over Bjork (U.S. Patent No. 6,474,475) in view of Sakurai (JP57015455).

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under 35 U.S.C. §§ 112, 102 and 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 1, 2 and 5-15 are currently in condition for allowance.

A. First Ground of Rejection:

As set forth above, in the Final Office Action, the Examiner rejected claims 1, 2, and 5-15 under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement.

1. **Clear legal precedent has been established regarding the enablement requirement of 35 U.S.C. § 112, first paragraph.**

Regarding the *enablement* requirement, the Examiner has the initial burden to establish a *reasonable basis* to question the enablement provided for the claimed invention. *In re Wright*, 999 F.2d 1557, 1562, 27 U.S.P.Q.2d 1510, 1513 (Fed. Cir. 1993). The test for enablement, as set forth by the Supreme Court, is whether the experimentation needed to practice the invention is undue or unreasonable. *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916). A patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661, 18 U.S.P.Q.2d 1331, 1332 (Fed. Cir. 1991). The *undue experimentation* test essentially evaluates whether one of reasonable skill in the art can make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *U.S. v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 U.S.P.Q.2d 1217, 1223 (Fed. Cir. 1988). As long as the specification discloses at least one method for making and using the claimed invention that bears a *reasonable correlation* to the entire scope of the claim, then the enablement requirement of Section 112 is satisfied. *In re Fisher*, 427 F.2d 833, 839, 166 U.S.P.Q. 18, 24 (C.C.P.A. 1970).

2. **The Examiner's rejection of claims 1, 2, and 5-15 for failing to comply with the enablement requirements of 35 U.S.C. § 112, first paragraph is improper.**

Independent claims 1 and 10 recite:

> [E]ach of the plurality of semiconductor die stacks include at least two semiconductor die coupled together by an adhesive and wherein the plurality of semiconductor die stacks *do not include a lead frame or a substrate.*
>
> (Emphasis added).

In rejecting independent claims 1 and 10, the Examiner stated the following:

> The definition of a substrate is a supporting material on or *in which* the components of an integrated circuit are *fabricated or attached*, or an insulating layer that components are formed on; therefore, since the dies contain circuits formed in semiconductor substrates the stack

> includes a substrate. Alternatively, the die stacks are formed on/attached to a holder albeit temporarily, and therefore the holder is still with the definition of a substrate. As such, the claim is not enabled, since one skilled in the art to which it pertains, or with which it is most nearly connected, cannot make a stack formed on *what it excludes*.
>
> Final Office Action, p. 2 (emphasis in original).

Regarding the enablement requirement of 35 U.S.C. § 112, first paragraph, Appellants assert that one of ordinary skill in the art would clearly understand how to form a die stack without a substrate based on the disclosure of the present application. Indeed, this concept is discussed throughout the application and distinguishes present embodiments from prior art in which packages are assembled by sequentially stacking die directly on a substrate. The Examiner's assertion that one of ordinary skill in the art would be confused about the meaning of the term "substrate" is unfounded. Indeed, Appellants assert that based on the context in which the term "substrate" is used and based on the customary meaning of the term in the art, one of ordinary skill in the art would clearly understand the intended meaning. Appellants assert that any confusion with respect to this claim feature merely arose because the Examiner attempted to provide his own definition for the term and that definition is unreasonably broad. Those skilled in the art would not make such an interpretation, nor would they be confused as to how to make or use the invention, as recited in the present claims.

First, the Examiner apparently asserted that a die stack inherently includes a substrate. *See* Final Office Action, page 2. This is clearly not the case. Indeed, the claim language set forth in claims 1 and 10, on its face, clearly indicates that the die stacks *do not include* substrates. Additionally, the specification clearly indicates that die stacks are eventually *stacked on* a substrate to form a package. They are not *integral with* the substrate. Further, the term "substrate" has a well known meaning in the art. Based on the context in which the term is utilized in the specification, one of ordinary skill in the art would readily discern the intended meaning. For example, the die stacks are

described as being coupled to the substrate to form a package, such as the packages illustrated in FIGS. 2 and 3 of the application. *See e.g.,* Application, page 18, lines 9-11. Prior to coupling the die stacks to the substrate, the die stacks do not include a substrate, and certainly do not form a package.

While it is true that integrated circuit dies are formed within or on a semiconductor material, those skilled in the art would not interpret an integrated circuit die or chip as including a substrate, semiconductor or otherwise. That is, those skilled in the art would not interpret a die or chip as having a substrate. This assertion by the Examiner has no technical basis and those skilled in the art would not reach this conclusion. Rather, as is clear from the present specification, those skilled in the art would fully appreciate that a semiconductor die is independent from a substrate.

Second, the Examiner apparently asserted that the temporary holder is a substrate. *See* Final Office Action, page 2. Again, this is clearly not the case. As set forth above, the term "substrate" has a well known meaning in the art. The definition that is apparently being asserted by the Examiner is unreasonably broad. Indeed, according to the Examiner it seems that anything on which a die stack is placed can be interpreted as a substrate. This clearly does not fit with the customary meaning of the term or the meaning of the term based on the context of its use throughout the present application. For example, as set forth in the present application, attaching a substrate to a die stack forms a package. *See e.g.,* Application, page 17, line 16 – page 18, line 11. However, when a die stack is placed on a temporary holding surface, a package is not formed. Attachment to a substrate is clearly understood by those skilled in the art to connote a permanent attachment, rather than a temporary placement.

In view of the remarks set forth above, Appellants assert that independent claims 1 and 10, as well as those claims dependent thereon, are fully compliant with the requirements of 35 U.S.C. § 112, first paragraph. Accordingly, Appellants request that

the Board overturn the Examiner's rejection of claims 1, 2, and 5-15 under 35 U.S.C. § 112, first paragraph.

B. **Second Ground of Rejection:**

As set forth above, in the Final Office Action, the Examiner rejected claims 1, 2, and 5-15 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement.

1. **Clear legal precedent has been established regarding the written description requirement 35 U.S.C. § 112, first paragraph.**

Regarding the *written description* requirement, the initial burden of proof regarding the sufficiency of the written description falls on the Examiner. Accordingly, the Examiner must present evidence or reasons why persons skilled in the art would not recognize a description of the claimed subject matter in the applicant's disclosure. *In re Wertheim*, 541 F.2d 257, 262, 191 U.S.P.Q. 90, 96 (CCPA 1976). The written description requirement does not require the claims to recite the same terminology used in the disclosure. The patentee may be his own lexicographer. *Ellipse Corp. v. Ford Motor Co.*, 171 U.S.P.Q. 513 (7th Cir. 1971), *aff'd.* 613 F.2d 775 (7th Cir. 1979), *cert. denied*, 446 U.S. 939 (1980). Moreover, any information contained in any part of the application as filed, including the specification, claims and drawings, may be added to other portions of the application without introducing new matter. Accordingly, if an application as originally filed contains a claim disclosing material not disclosed in the remainder of the specification, the applicant may amend the specification to include the claimed subject matter. *In re Benno*, 768 F.2d 1340, 226 U.S.P.Q. 683 (Fed. Cir. 1985).

2. **The Examiner's rejection of claims 1, 2, and 5-15 for failing to comply with the written description requirements of 35 U.S.C. § 112, first paragraph is improper.**

Independent claims 1 and 10 recite:

> [E]ach of the plurality of semiconductor die stacks include at least two semiconductor die coupled together by an adhesive

> and wherein the plurality of semiconductor die stacks *do not include a lead frame or a substrate*.
>
> (Emphasis added).

In rejecting independent claims 1 and 10, the Examiner stated the following:

> There is no support in the specification for the negative limitation that the die stacks do not include a lead frame.
>
> Final Office Action, p. 3.

Appellants assert that the present application complies with the written description requirement of 35 U.S.C. § 112, first paragraph. Specifically, Appellants assert that sufficient support is provided in the specification for the negative limitation that the die stacks do not include a lead frame. For example, numerous times throughout the application a die is explicitly described as being coupled merely to other die and not to a substrate. *See e.g.,* Application, page 17, line 16 – page 18, line 11. While Appellants concede that a lead frame is different than a substrate, the indication by the present specification that the die stack is not coupled to a substrate is sufficient to indicate that the die stack is not coupled to a lead frame either since those skilled in the art would appreciate that attachment to a lead frame is simply an alternative to attachment of the dies to a substrate. One of ordinary skill in the art would recognize this. Further, FIGS. 5A, 5B, 5C, and 5D all illustrate die stacks that are not coupled to a lead frame. The point is that the die stacks are formed before attachment to a permanent surface, such as a substrate or lead frame, for formation of a package. Those skilled in the art would clearly recognize the description of the recited subject matter to exclude attachment of the die stack to a lead frame.

In view of the remarks set forth above, Appellants assert that independent claims 1 and 10, as well as those claims dependent thereon, are fully compliant with the requirements of 35 U.S.C. § 112, first paragraph. Accordingly, Appellants request that the Board overturn the Examiner's rejection of claims 1, 2, and 5-15 under 35 U.S.C. § 112, first paragraph.

C. **Third Ground of Rejection:**

As set forth above, in the Final Office Action, the Examiner rejected claims 1, 2, and 5-15 under 35 U.S.C. § 112, second paragraph as failing to comply with the enablement requirement.

1. **Clear legal precedent has been established regarding 35 U.S.C. § 112, second paragraph.**

In ruling on a claim of patent indefiniteness, a court must determine whether those skilled in the art would understand what is claimed when the claim is read in light of the specification. *Personalized Media Communications, Inc. v. Int'l Trade Comm'n*, 161 F.3d 696, 705, 48 U.S.P.Q.2d 1880 (Fed. Cir. 1998); *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 U.S.P.Q.2d 1081 (Fed. Cir. 1986). A claim in not indefinite merely because it poses a difficult issue of claim construction; if the claim is subject to construction, i.e., it is not insolubly ambiguous, it is not invalid for indefiniteness. *Honeywell Int'l, Inc. v. Int'l Trade Comm'n*, 341 F.3d 1332, 1338-39, 68 U.S.P.Q.2d 1023 (Fed. Cir. 2003). That is, if the meaning of the claim is discernible, even though the task may be formidable and the conclusion may be one over which reasonable persons disagree, a claim is sufficiently clear to avoid invalidity on indefiniteness grounds. *Exxon Research & Eng'g Co. v. United States*, 265 F.3d 1371, 1375, 60 U.S.P.Q.2d 1272 (Fed. Cir. 2001). The failure to define a term is not fatal; if the meaning of the term is fairly inferable from the patent, an express definition is not necessary. *Bancorp Services LLC v. Hartford Life Insurance Co.*, 69 U.S.P.Q.2d 1996, 2000 (Fed. Cir. 2004). Even though an entire term is not defined in a patent or industry publications, individual components of the phrase may have well-recognized meanings to those of skill in art and a reader can infer the meaning of the entire phrase with reasonable confidence. *Id.*

Regarding functional limitations, the Examiner must evaluate and consider the functional limitation, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. *See*

M.P.E.P. § 2173.05(g); *In re Swinehart*, 169 U.S.P.Q. 226, 229 (C.C.P.A. 1971); *In re Schreiber*, 44 U.S.P.Q.2d 1429, 1432 (Fed. Cir. 1997). If the Examiner believes the functional limitation to be inherent in the cited reference, then the Examiner "must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art." *Ex parte Skinner,* 2 U.S.P.Q.2d 1788, 1789 (Bd. Pat. App. & Inter. 1986).

2. **The Examiner's rejection of claims 1, 2, and 5-15 under 35 U.S.C. § 112, second paragraph for failing to particularly point out and distinctly claim the subject matter regarded as the invention is improper.**

Independent claim 1 recites:

> A holder having a plurality of semiconductor die stacks thereon, the holder *configured to temporarily hold the plurality of semiconductor die stacks.*
>
> (Emphasis added).

Independent claim 10 recites:

> A tape reel having a plurality of semiconductor die stacks thereon, the tape reel *configured to temporarily hold the plurality of semiconductor die stacks.*
>
> (Emphasis added).

In rejecting independent claims 1 and 10, the Examiner stated the following:

> The term "configured," while applicant's specification makes mention of the configuration of chips (e.g., different sizes etc.) it is completely silent as to how the "holder is *configured* ..." except to say, "[t]he holding surface is considered temporary in that the wafer itself may be used to temporarily hold, transfer, test or store one or more die stacks *for example*." There is nothing in the specification that would apprise one of the metes and bounds of how the substrate was configured or the structural limitations imparted.
>
> Final Office Action, p. 3 (emphasis in original).

Additionally, in a footnote, the Examiner stated:

> Note, a substrate/PCB that a chip is soldered may be considered temporary in that the chip may be removed (e.g., defect in chip).
>
> Final Office Action, pp. 2-3 (error in original).

As set forth in the specification and throughout the prosecution history, embodiments of the present invention distinguish over the prior art, in part, because a die stack is formed prior to attaching the die stack on a substrate. In other words, after the die stack is formed, it exists separate from the substrate. Thus, the die stack may be positioned on a temporary holding surface (e.g., film frame, gel pack, tape reel, or JEDEC tray) before removing the die stack and coupling it to a substrate to form a package. In contrast, prior art die stacking techniques begin by stacking die directly on a substrate. Accordingly, the prior art merely includes die stacks that include a substrate since the die stacks are formed directly on the substrate. It should be clear from this explicitly noted contrast between the prior art and the present invention that a holding surface *configured to temporarily hold the plurality of semiconductor die stacks* is a surface that allows the die stacks to be readily removed for coupling to a substrate. For example, the temporary holding surface may allow ready removal with a stacking tip or removal via separation of an individual die, if the temporary holding surface is a die wafer. Appellants note that "configured" is commonly used in claims and is well understood to refer to elements that are sized, arranged or manufactured to form a specified structure or achieve a specified result. In this case, the holder is sized, arranged or manufactured to temporarily hold a die stack. The meaning is clear and the context and usage of the terminology would be readily ascertainable by those skilled in the art. Therefore the claim is fully compliant with 35 U.S.C. § 112, second paragraph

Further, contrary to the Examiner's assertions, the temporary holding surface is certainly not a substrate to which a die stack is soldered. This would clearly be an unreasonable interpretation. While parts that are soldered to other parts can indeed be

separated, the purpose of a solder connection is to permanently attach the parts together. According to the Examiner any type of surface or connection would apparently be "temporary," if the connection could ever be severed or destroyed. This again is not a reasonable interpretation, nor is it one that those skilled in the art would make.

In view of the remarks set forth above, Appellants assert that independent claims 1 and 10, and those claims dependent thereon, are fully compliant with the requirements of 35 U.S.C. § 112, second paragraph. Accordingly, Appellants request that the Board overturn the Examiner's rejection of claims 1, 2, and 5-15 under 35 U.S.C. § 112, second paragraph.

D. **Fourth Ground of Rejection:**

As set forth above, in the Final Office Action, the Examiner rejected claims 1, 5-9, and 11 under 35 U.S.C. § 103(a) as being obvious over Sakurai (JP57015455) in view of Ang et al. (U.S. Patent No. 6,599,764).

1. **Clear legal precedent has been established regarding 35 U.S.C. § 103.**

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (P.T.O. Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (Bd. Pat. App. & Inter. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc.*

v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Moreover, the Examiner must provide objective evidence, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to combine or modify the cited references. *In re Lee*, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002).

It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983); M.P.E.P. § 2145. Moreover, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); see M.P.E.P. § 2143.01. One important indicium of nonobviousness is "teaching away" from the claimed invention by the prior art or by experts in the art at or after the time the invention was made. *U.S. v. Adams*, 383 U.S. 39, 148 U.S.P.Q. 479 (1966).

2. **The Examiner's rejection of claims 1, 5-9, and 11 under 35 U.S.C. § 103(a) is improper.**

Independent claims 1 and 10 recite:

> [E]ach of the plurality of semiconductor die stacks include at least two semiconductor die coupled together by an adhesive and wherein the plurality of semiconductor die stacks *do not include a lead frame or a substrate*.
>
> (Emphasis added).

In rejecting independent claim 1, the Examiner stated the following:

> Sakurai (Fig. 1, 2) discloses:
>
> (cl. 1) a plurality of semiconductor die stacks thereon (1a-c), wherein each of the plurality of semiconductor die stacks include at least two semiconductor die coupled together by an adhesive (6) and wherein the plurality of

> semiconductor die stacks do not include a lead frame (e.g. none shown) or an interposing substrate;
> (cl. 6) bottom two dies have an extent from left surface to its opposite right surface and therefore thickness larger than top die;
> (cl. 7) where the topside of at least one die is less than topside of a second die (Fig. 2);
> cl. 5, 11) at least three dies connected by adhesives (Fig. 2)
>
> Sakurai fails to explicitly disclose a temporary holder or that at least on die is memory.
>
> Ang utilizes a temporary holder (100) for dies and at least on die being memory (e.g. Col. 4, Line 10).
>
> It would have been obvious to one of ordinary skill in the art to incorporate use of a temporary holder and memory die as taught by Ang with the die stack of Sukurai in order to provide a die and testing means as taught by Ang (Title) and as required by Sakurai (Abstract).

Final Office Action, p. 4.

Additionally, in a footnote, the Examiner stated:

> Note, alternatively Vindasius (U.S. 5,891,761) requiring that its die-stack be tested in combination with any test board, such as Hiruta et al. (U.S 6,094,057) providing a testing means could have been used to evidence the obviousness of the claimed invention.
>
> E.g. same as shown by applicant's Figure 5b.

Final Office Action, page 4.

First, Appellants assert that it is improper for the Examiner to rely on an abstract rather than the underlying document itself, particularly in the case of foreign language references. *See Ex parte Jones*, 62 U.S.P.Q.2d 1206 (PTO Bd. App. 2001); see M.P.E.P. § 706.02. As noted by the Board of Patent Appeals and Interferences, the reliance on abstracts is problematic, because abstracts are often prone to erroneous or incomplete

descriptions of the invention. "A proper examination under 37 C.F.R. § 1.104 should be based on the underlying documents and translations, where needed." *Id.* As set forth in Section 706.02 of the Manual of Patent Examining Procedure, if a prior art reference is in a language other than English and the Examiner seeks to rely on that document, a translation *must* be obtained so that the record is clear as to the precise facts the Examiner is relying on in support of the rejection. In view of the Examiner's reliance on the Sakurai reference, Appellants assert that the Examiner's rejection of claims 1, 5-9 and 11 under 35 U.S.C. § 103(a) is improper.

Further, Appellants assert that even assuming *arguendo* that the Sakurai reference teaches what the Examiner alleges that it teaches, it cannot be combined with the Ang reference. As set forth above, claim 1 recites that the plurality of semiconductor die stacks *do not include a lead frame or a substrate*. In stark contrast, Ang requires a substarte 104 to connect the die stack (406 and 408) to the test board 100. For example, Ang teaches that the test platform 100 is a single board configured to receive a multi-die *package* 102. The package includes a first die 106, a second die 108 and *the substrate 104*. Indeed, every relevant figure in the Ang reference illustrates the die coupled to a substrate. Accordingly, the Ang reference teaches away from the present invention. Further, any theoretical combination of the Ang reference with the Sakurai reference would necessarily include a substrate.

In view of the remarks set forth above, Appellants assert that independent claim 1 is allowable. For similar reasons, independent claim 10 is also believed to be allowable. Accordingly, Appellants request that the Board overturn the Examiner's rejection of claims 1, 5-9, and 11 under 35 U.S.C. § 103(a).

E. **Fifth Ground of Rejection:**

The Examiner rejected claim 1 under 35 U.S.C. § 103(a) as being obvious over Bjork (U.S. Patent No. 6,474,475) in view of Sakuri (JP57015455).

1. **Clear legal precedent has been established regarding 35 U.S.C. § 103.**

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (P.T.O. Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (Bd. Pat. App. & Inter. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Moreover, the Examiner must provide objective evidence, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to combine or modify the cited references. *In re Lee*, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002).

It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983); M.P.E.P. § 2145. Moreover, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); see M.P.E.P. § 2143.01. One important indicium of nonobviousness is "teaching away" from the claimed invention by the prior art or by experts in the art at or after the time the invention was made. *U.S. v. Adams*, 383 U.S. 39, 148 U.S.P.Q. 479 (1966).

2. **The Examiner's rejection of claim 1 under 35 U.S.C. § 103(a) is improper.**

Independent claim 1 recites:

> A holder having a plurality of semiconductor die stacks thereon, the holder configured to temporarily hold the plurality of semiconductor die stacks, wherein each of the plurality of semiconductor die stacks include at least two semiconductor die *coupled together by an adhesive* and wherein the plurality of semiconductor die stacks *do not include a lead frame or a substrate*.
>
> (Emphasis added).

In rejecting independent claim 1, the Examiner stated the following:

> Bjork (Fig. 1, 3) discloses:
>
> (cl. 1) a holder (12) having a plurality of semiconductor die stacks thereon (40), configured (see footnote 1) to temporarily hold (e.g. carrier) the plurality of die stack wherein each of the plurality of semiconductor die stacks include a least two semiconductor die coupled together (e.g. both "affixed" to layer, 60) and wherein the plurality of semiconductor die stacks do not include a lead frame (e.g. leads detached from frame) or permanent substrate.
>
> Bjork does not appear to explicitly disclose use of an adhesive.
>
> However, Sakurai utilizes an adhesive (6).
>
> It would have been obvious to one of ordinary skill in the art to incorporate use of an adhesive with the dies in order to affix or secure them as taught to an adjacent material as taught by Sakurai (Eng. Abstract).

Final Office Action, pp. 5-6.

First, as set forth above, Appellants assert that it is improper for the Examiner to rely on an abstract rather than the underlying document itself, particularly in the case of

foreign language references. *See Ex parte Jones*, 62 U.S.P.Q.2d 1206 (PTO Bd. App. 2001); see M.P.E.P. § 706.02. As noted by the Board of Patent Appeals and Interferences, the reliance on abstracts is problematic, because abstracts are often prone to erroneous or incomplete descriptions of the invention. "A proper examination under 37 C.F.R. § 1.104 should be based on the underlying documents and translations, where needed." *Id.* As set forth in Section 706.02 of the Manual of Patent Examining Procedure, if a prior art reference is in a language other than English and the Examiner seeks to rely on that document, a translation *must* be obtained so that the record is clear as to the precise facts the Examiner is relying on in support of the rejection. In view of the Examiner's reliance on the Sakurai reference, Appellants assert that the Examiner's rejection of claims 1, 5-9 and 11 under 35 U.S.C. § 103(a) is improper.

Second, Appellants assert that the individual I/C devices 42 and 44 of the Bjork reference would not be considered "die stacks," as presently recited. Indeed, as the Examiner essentially admitted, the Bjork reference fails to disclose that the semiconductor die are *coupled together by an adhesive*. The Examiner attempted to remedy this admitted deficiency in the Bjork reference by citing the Sakurai reference. However, even if the Sakurai reference teaches what the Examiner alleges it teaches, the I/C devices 42 and 44 of the Bjork reference are separated from each other by either lead protection elements 60 or the leads 52 and 54 themselves. *See* Bjork, col. 5, lines 21-25; FIGS. 2 and 3. Thus, the I/C devices 42 and 44 are actually *prevented* from being coupled together by an adhesive. Accordingly, in order for the IC devices 42 and 44 to be coupled together by adhesive, the lead protection elements 60 would have to be removed and the leads 52 and 54 would have to be removed or bent. This would clearly destroy the function of the lead protection elements 60 and/or the leads 52 and 54. In other words, it would change the principle of operation of the invention described in the Ang reference. Accordingly, the Ang reference teaches away from both the present invention and the hypothetical combination with the Bjork reference suggested by the Examiner.

In view of the remarks set forth above, Appellants assert that independent claim 1 is allowable. Accordingly, Appellants request that the Board overturn the Examiner's rejection of claim 1under 35 U.S.C. § 103(a).

Conclusion

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: March 19, 2007

W. Allen Powell
Reg. No. 56,743
FLETCHER YODER
P.O. Box 692289
Houston, TX 77269-2289
(281) 970-4545

8. APPENDIX OF CLAIMS ON APPEAL

Listing of Claims:

1. A holder having a plurality of semiconductor die stacks thereon, the holder configured to temporarily hold the plurality of semiconductor die stacks, wherein each of the plurality of semiconductor die stacks include at least two semiconductor die coupled together by an adhesive and wherein the plurality of semiconductor die stacks do not include a lead frame or a substrate.

2. The holder, as set forth in claim 1, comprising a tape reel having the plurality of semiconductor die stacks thereon.

5. The holder, as set forth in claim 1, wherein each of the plurality of semiconductor die stacks comprises at least three semiconductor die, each of the semiconductor die being coupled together by the adhesive.

6. The holder, as set forth in claim 1, wherein one of the at least two semiconductor die is thicker than a second of the at least two semiconductor die.

7. The holder, as set forth in claim 1, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

8. The holder, as set forth in claim 1, wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

9. The holder, as set forth in claim 1, wherein at least one of the at least two semiconductor die comprises a memory die.

10. A tape reel having a plurality of semiconductor die stacks thereon, the tape reel configured to temporarily hold the plurality of semiconductor die stacks, wherein each of the plurality of semiconductor die stacks include at least two semiconductor die coupled together by an adhesive and wherein the plurality of semiconductor die stacks do not include a lead frame or a substrate.

11. The tape reel, as set forth in claim 10, wherein each of the plurality of semiconductor die stacks comprises at least three semiconductor die, each of the semiconductor die being coupled together by the adhesive.

12. The tape reel, as set forth in claim 10, wherein one of the at least two semiconductor die is thicker than a second of the at least two semiconductor die.

13. The tape reel, as set forth in claim 10, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

14. The tape reel, as set forth in claim 10, wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

15. The tape reel, as set forth in claim 10, wherein at least one of the at least two semiconductor die comprises a memory die.

9. EVIDENCE APPENDIX

None.

10. RELATED PROCEEDINGS APPENDIX

None.